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1	(sta static with timing with anal\$6) and (dummy test\$4) with clock with (edge transition\$4 ris\$4 fall\$4)
2	(dummy test\$4) with clock with (switch\$4 edge transition\$4 ris\$4 fall\$4) and (timing with (evaluat\$4 anal\$6 simulat\$4 synthes\$6))
3	(dummy test\$4) with clock with (switch\$4 edge transition\$4 ris\$4 fall\$4) and (timing with (evaluat\$4 anal\$6 simulat\$4 synthes\$6)) and (edge polarit\$4 sense state) same (inver\$4 conver\$4) same (opposit\$5 (negative and positive) direction)
4	(dummy test\$4) with clock with (switch\$4 edge transition\$4 ris\$4 fall\$4) and (timing with (evaluat\$4 anal\$6 simulat\$4 synthes\$6)) and (edge polarit\$4 sense state) same (chang\$4 conver\$4 transform\$4) same (inver\$\$ opposit\$5 (negative and positive) direction)
5	(dummy test\$4) with clock with (switch\$4 edge transition\$4 ris\$4 fall\$4) and (timing with (evaluat\$4 anal\$6 simulat\$4 synthes\$6)) and (edge polarit\$4 sense state) same (chang\$4 conver\$4 transform\$4) same (inver\$\$ opposit\$5 (negative and positive) direction) and "716"/\$.ccls.
6	slack with (comput\$5 adjust\$5) and clock with (test\$4 dummy)
7	slack with (comput\$5 adjust\$5) and clock with (test\$4 dummy) and timing with anal\$6
8	(edge polarity sense) same (opposit\$5 inver\$\$) and (slack with (calculat\$5 comput\$5 adjust\$5)) and clock with (test\$4 dummy) and timing with anal\$6